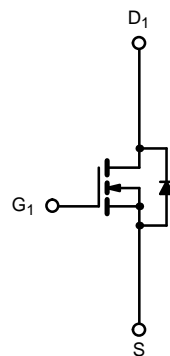
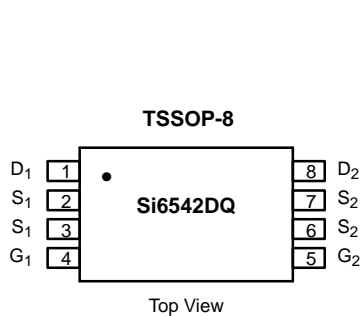


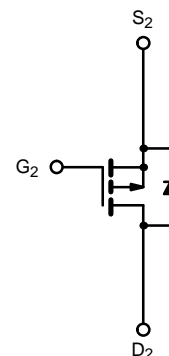


Dual N- and P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY			
	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	20	0.09 @ $V_{GS} = 10$ V	± 2.5
		0.175 @ $V_{GS} = 4.5$ V	± 1.8
P-Channel	-20	0.17 @ $V_{GS} = -10$ V	± 1.9
		0.32 @ $V_{GS} = -4.5$ V	± 1.3



N-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	V_{DS}	20	-20	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	± 2.5	A
		$T_A = 70^\circ\text{C}$	± 2.0	
Pulsed Drain Current	I_{DM}	± 20	± 15	A
Continuous Source Current (Diode Conduction) ^a	I_S	1.25	-1.25	A
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	1.0	W
		$T_A = 70^\circ\text{C}$	0.64	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	125	$^\circ\text{C}/\text{W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

For SPICE model information via the Worldwide Web: <http://www.vishay.com/www/product/spice.htm>



SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)								
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit		
Static								
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	1.0			V	
		V _{DS} = V _{GS} , I _D = -250 μA	P-Ch	-1.0				
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V	N-Ch			1	μA	
		V _{DS} = -20 V, V _{GS} = 0 V	P-Ch			-1		
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 55 °C	N-Ch			25		
		V _{DS} = -20 V, V _{GS} = 0 V, T _J = 55 °C	P-Ch			-25		
On-State Drain Current ^a	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	N-Ch	14			A	
		V _{DS} = -5 V, V _{GS} = -10 V	P-Ch	-10				
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 2.5 A	N-Ch		0.065	0.09	Ω	
		V _{GS} = -10 V, I _D = 1.9 A	P-Ch		0.13	0.17		
		V _{GS} = 4.5 V, I _D = 1.8 A	N-Ch		0.100	0.175		
		V _{GS} = -4.5 V, I _D = 1.3 A	P-Ch		0.26	0.32		
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 2.5 A	N-Ch		5		S	
		V _{DS} = -15 V, I _D = -1.9 A	P-Ch		3			
Diode Forward Voltage ^a	V _{SD}	I _S = 1.25 A, V _{GS} = 0 V	N-Ch		0.8	1.2	V	
		I _S = -1.25 A, V _{GS} = 0 V	P-Ch		0.8	-1.2		
Dynamic^b								
Total Gate Charge	Q _g	N-Channel V _{DS} = 10 V, V _{GS} = 10 V, I _D = 2.5 A P-Channel V _{DS} = -10 V, V _{GS} = -10 V, I _D = -1.9 A	N-Ch		7	10	nC	
Gate-Source Charge	Q _{gs}		N-Ch		0.9			
Gate-Drain Charge	Q _{gd}		P-Ch		1.3			
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 10 V, R _L = 10 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω P-Channel V _{DD} = -10 V, R _L = 10 Ω I _D ≅ -1 A, V _{GEN} = -10 V, R _G = 6 Ω	N-Ch		11	20	ns	
Rise Time	t _r		P-Ch		9	20		
Turn-Off Delay Time	t _{d(off)}		N-Ch		11	20		
			P-Ch		12	25		
Fall Time	t _f		N-Ch		16	30		
			P-Ch		17	30		
Source-Drain Reverse Recovery Time	t _{rr}		I _F = 1.25 A, di/dt = 100 A/μs	N-Ch		45		70
			I _F = -1.25 A, di/dt = 100 A/μs	P-Ch		35		70

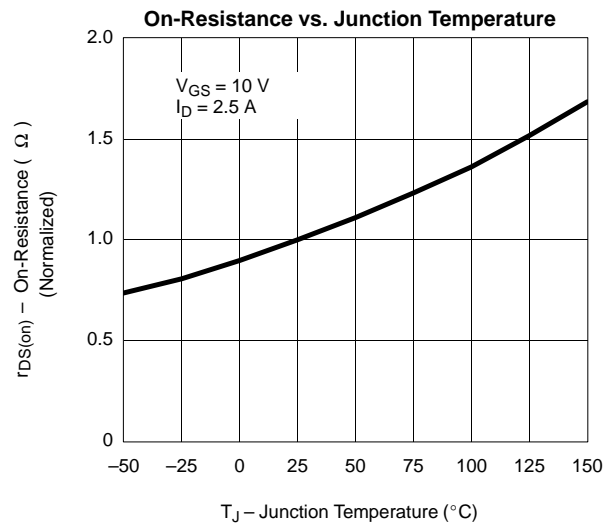
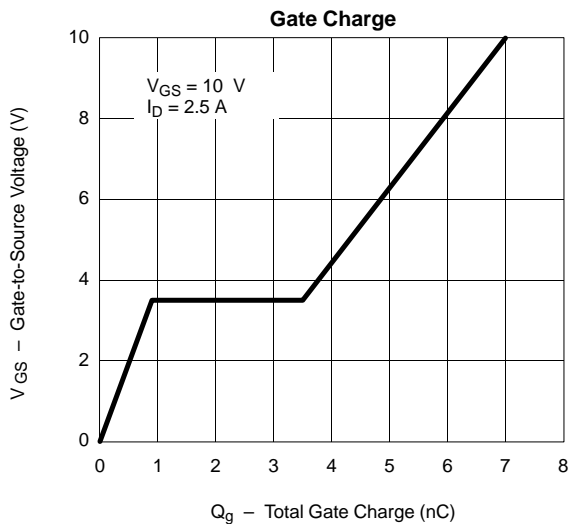
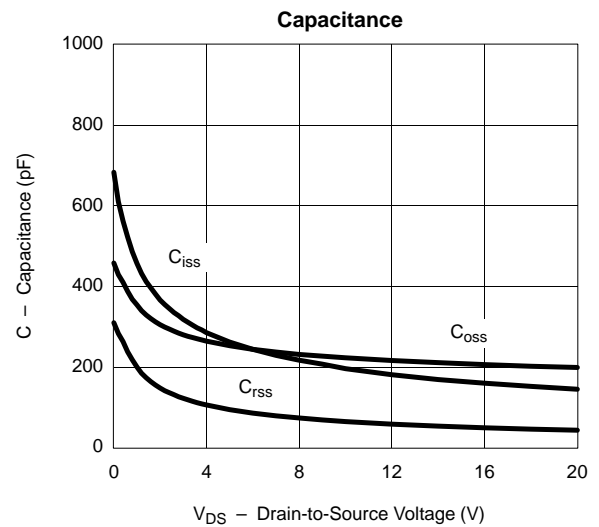
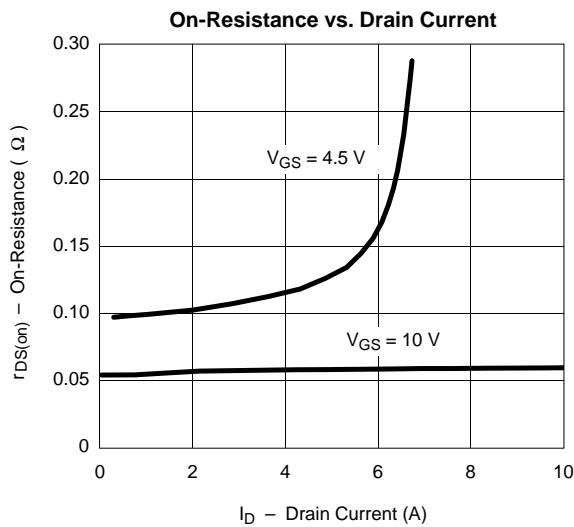
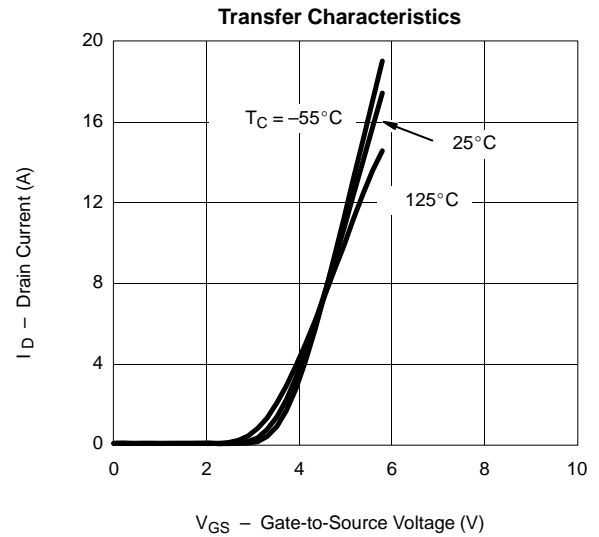
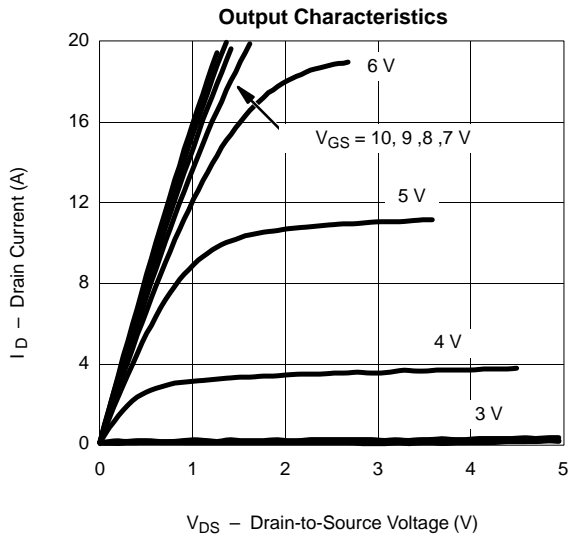
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

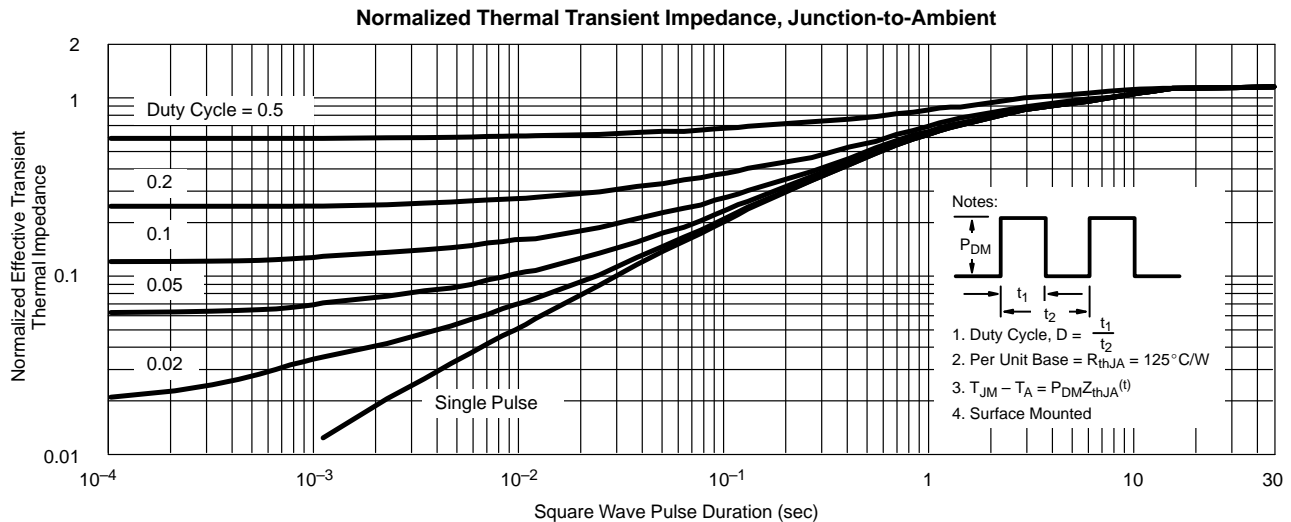
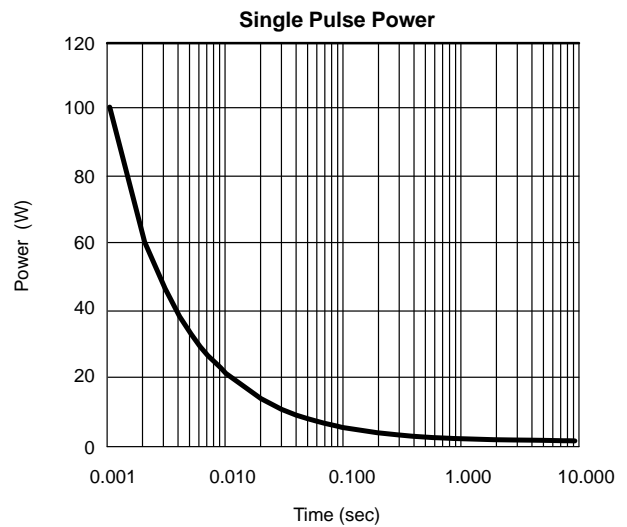
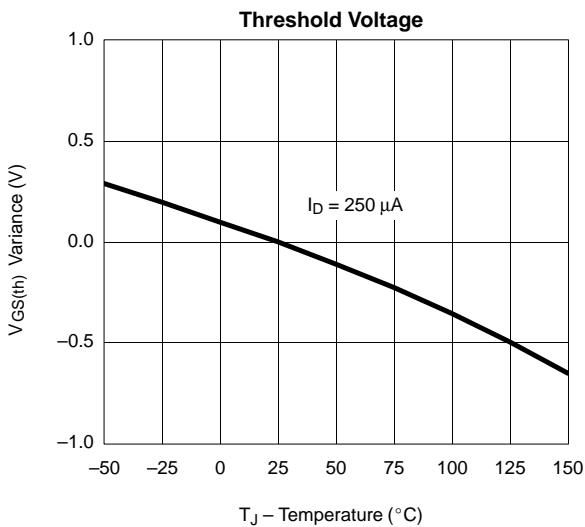
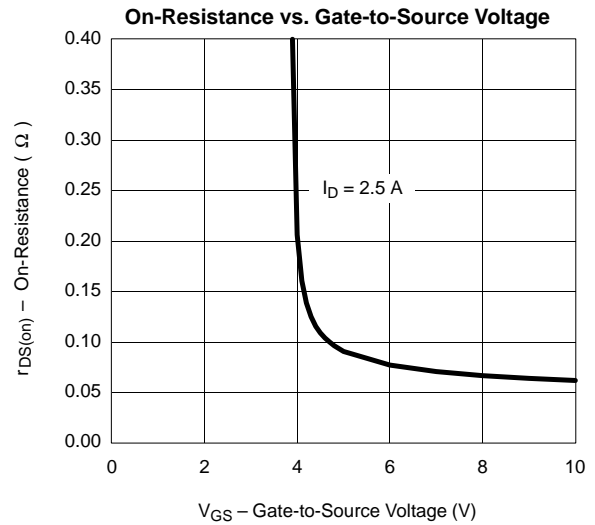
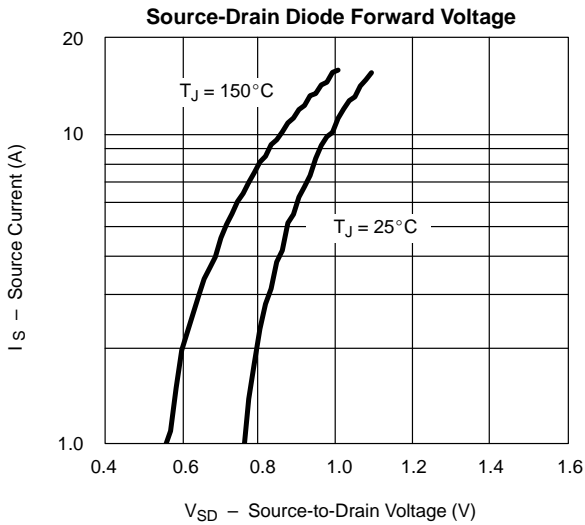


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

N-CHANNEL



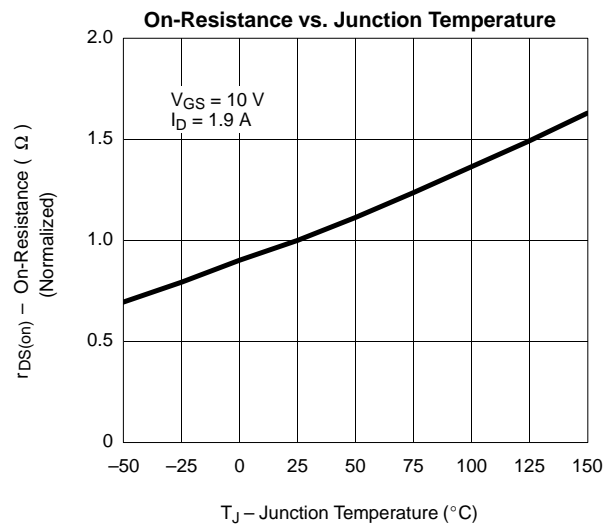
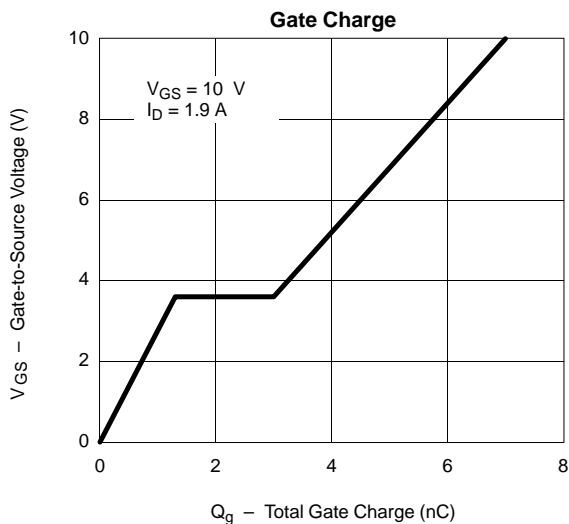
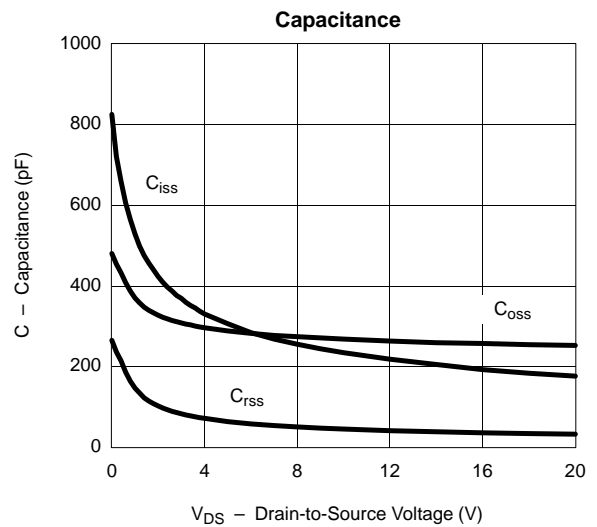
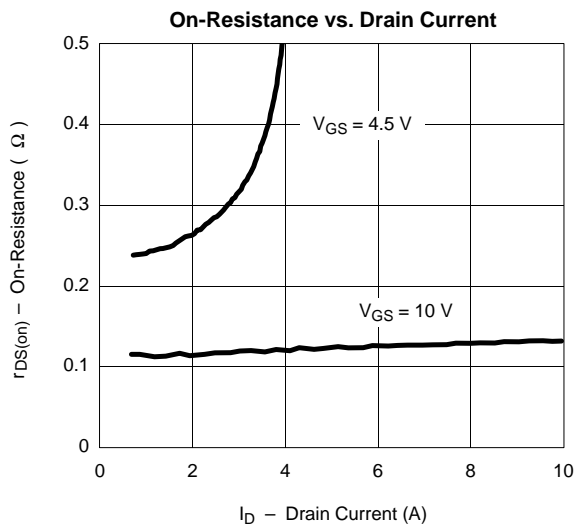
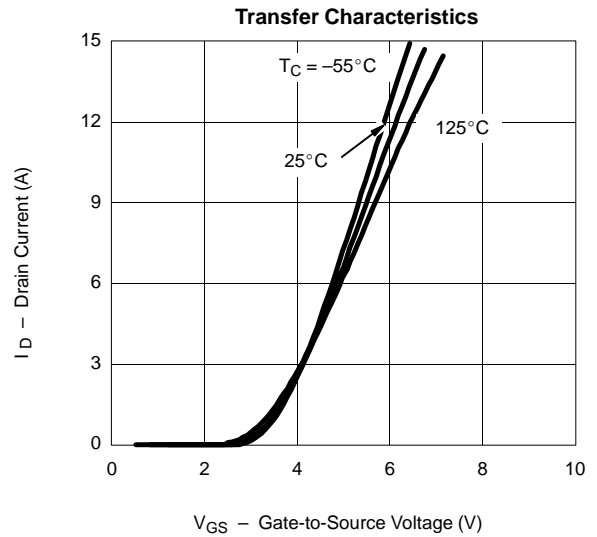
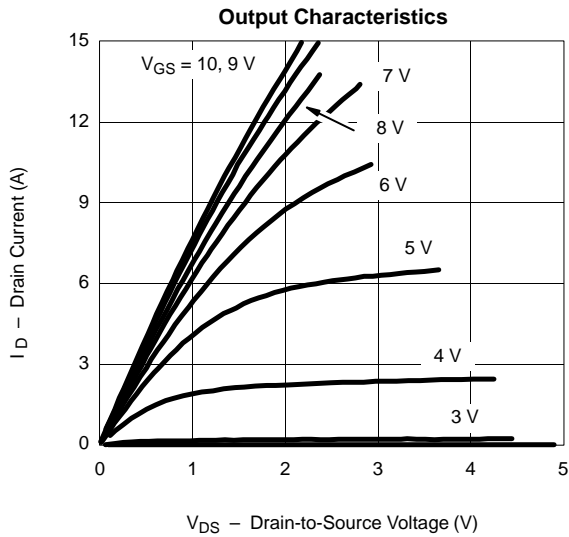
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) N-CHANNEL





TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

P-CHANNEL



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) P-CHANNEL

